embodiments. Collector **34** and emitter **36** may be formed simultaneously, and hence may be at a same level, have a same concentration, and/or may extend down to substantially a same depth. Base pick-up region **32**, collector **34**, and emitter **36** may be spaced apart from each other by isolation regions **40**, which may be shallow trench isolation (STI) regions. HVPW **24** may form a ring surrounding BJT **52** (also refer to FIGS. **2**A and **2**B), and electrically isolates BJT **52** from external devices. P-type ring **42**, which may be a heavily doped p-type region, may be formed at a top surface of HVPW **24**.

[0017] N− region (a moderately doped n-type region) **44** is formed under emitter **36**, with at least a portion of N− region **44** vertically overlapping at least a portion, and possibly an entirety, of emitter **36**. Furthermore, the top surface of N− region **44** contacts the bottom surface of emitter **36**. N− region **44** may, or may not, extend to directly under and vertically overlapping a portion of the neighboring STI regions **40**. N− region **44** has a net n-type impurity concentration higher than the n-type impurity concentration of HVNW **26**. In an exemplary embodiment, a ratio of the n-type impurity concentration of N− region **44** to the impurity concentration of HVNW **26** is greater than about 5, or greater than about 10, 20, or even about 100. Furthermore, the n-type impurity concentration of N− region **44** is lower than the impurity concentrations of emitter **36** and collector **34**. In an exemplary embodiment, a ratio of the impurity concentration of N− region **44** to the impurity concentration of emitter **36** is smaller than about ⅕, or smaller than about 1/10, 1/20, or even about 1/100. HVNW **26** includes region **26**A, which has a side edge forming interface **48** with a side edge of N− region **44**, and the impurity concentration of N− region **44** is also greater than that of region **26**A. Interface **48** may be substantially perpendicular to major surfaces of substrate **20**, such as surface **20**A.

[0018] Optionally, P− region (a moderately doped p-type region) **46** is formed under collector **34**, with at least a portion of P− region **46** vertically overlapping at least a portion, and possibly an entirety, of collector **34**. P− region **46** may space HVNW **26** apart from collector **34**. Furthermore, the top surface of P− region **46** contacts the bottom surface of collector **34**. N− region **44** and P− region **46** may be at substantially a same level. P− region **46** may, or may not, extend to directly under the neighboring STI regions **40**. P− region **46** has a net p-type impurity concentration higher than the n-type impurity concentration of HVNW **26**. In an exemplary embodiment, a ratio of the p-type impurity concentration of P− region **46** to the n-type impurity concentration of HVNW **26** is greater than about 5, or greater than about 10, 20, or even 100. Furthermore, the p-type impurity concentration of P− region **46** is lower than the impurity concentrations of collector **34** and emitter **36**. In an exemplary embodiment, a ratio of the p-type impurity concentration of P− region **46** to the impurity concentration of collector **34** is smaller than about ⅕, or smaller than about 1/10, about 1/20, or even about 1/100. HVNW **26** includes region **26**A, which has a side edge forming interface **50** with a side edge of P− region **46**, and the impurity concentration of P− region **46** is also greater than that of region **26**A of HVNW **26**. Interface **50** may be substantially perpendicular to major surfaces of substrate **20**, such as surface **20**A.

[0019] Horizontal spacing S between interfaces **48** and **50** affects the performance of ESD device **30**, wherein spacing S is measured in a direction parallel to a major surface (such as surface **20**A) of substrate **20**. FIG. **3** illustrates the simulation results that reveal the relationship between triggering voltage Vt**1** of ESD device **30** and spacing S, wherein spacing S is a relative value. The triggering voltage Vt**1** is the voltage at which ESD device **30** breaks down to conduct ESD currents. It is observed that with the increase in spacing S, triggering voltage Vt**1** increases. Although not illustrated, holding voltages of ESD device **30** follow the similar trend as that of triggering voltage Vt**1**, and with the increase in spacing S, the holding voltage increases.

[0020] FIG. **4** illustrates a schematic illustration of the holding voltage Vh and triggering voltage Vt**1**. According to FIG. **3**, increasing spacings S for the ESD devices may cause the corresponding design window (the window between holding voltage Vh and triggering voltage Vt**1**) to shift to higher voltages, and reducing spacings S for the ESD devices may cause the corresponding design window to shift to lower voltages. If two circuits in the same chip require different design windows to suit to different power supply voltages VDD and different breakdown voltages of the respective internal circuits, then two ESD devices **30** may be formed on the same chip, with spacings S of two ESD devices **30** be adjusted to different values.

[0021] N− region **44** may be formed by implanting into HVNW **26**. Further, N− region **44** may be formed simultaneously with the formation of the N− regions of other devices in the same chip, such as the N− regions of low-voltage devices. P− region **46** may also be formed by implanting into HVNW **26**, and may be formed simultaneously with the formation of the P− regions of other devices in the same chip, such as the P− regions of low-voltage devices. Accordingly, no additional process steps and no additional cost are needed for forming N− region **44** and P− region **46**.

[0022] In FIG. **1**A, N− regions **44** and P− region **46** extend to directly underlying the neighboring STI regions **40**. Accordingly, the horizontal dimensions W**1** and W**2** of N− region **44** and P− region **46** are greater than the respective horizontal dimensions W**3** and W**4** of the respective overlying emitter **36** and collector **34**. FIGS. **1**B and **1**C illustrate alternative embodiments. In FIG. **1**B, the edges of N− region **44** and P− region **46** are aligned to the side edges of the respective emitter **36** and collector **34**. Accordingly, the horizontal dimensions W**1** and W**2** of N− region **44** and P− region **46** are substantially equal to the respective horizontal dimensions W**3** and W**4** of the respective overlying emitter **36** and collector **34**. In FIG. **1**C, the horizontal dimensions W**1** and W**2** of N− region **44** and P− region **46** are smaller than the respective dimensions W**3** and W**4** of the respective overlying emitter **36** and collector **34**. Accordingly, N− region **44** and P− region **46** vertically overlap portions, but not all, of the respective overlying emitter **36** and collector **34**.

[0023] ESD device **30** may have various designs with different top views. For example, FIG. **2**A illustrates a top view in accordance with an embodiment. Collectors **34** (which are interconnected to each other) and emitters **36** (which are interconnected to each other) of the same ESD device **30** include parallel strips placed in an alternating pattern. In this exemplary embodiment, the outmost strips near base **32** are collectors **34**, and base pick-up region **32** may form a ring encircling collector strips **34** and emitter strips **36**. In alternative embodiments, as shown in FIG. **2**B, the outmost strips near base **32** are emitters **36**. The performance of the embodiment in which the outmost strips are collectors **34** may be essentially the same as the embodiments in which the outmost strips are emitters **36**. Furthermore, HVPW **24** may form